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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,712	03/18/2004	Rafael Camarota	015114-069900US	7512

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/804,712	CAMAROTA ET AL.
	Examiner	Art Unit
	Quan Tra	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 17-19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii et al. (US 2002/0017940).

Fujii et al.'s discloses in figure 5 an electronic system comprising: a first integrated circuit comprising: an input buffer (4-6) coupled between a first supply terminal and a second supply terminal and further coupled to receive an input signal on a pad (1); and a clamp diode (2a) coupled between the pad and the first supply terminal; and a resistor (7) coupled to the pad, and further coupled to receive an input signal.

As to claim 2, it is inherent that there is a second integrated circuit (circuit, not shwin, that generating signal to node 1) coupled to the resistor and to provide the input signal.

As to claim 3, figure 5 shows that the clamp diode has a anode and a cathode, the anode is coupled to the pad, and the cathode is coupled to the first supply terminal.

As to claim 4, figure 5 shows that the first supply terminal is configured to receive a positive supply voltage, and the second supply voltage is configured to receive a ground supply.

As to claim 5, figure 5 shows that the integrated circuit further comprises: a pull-up output device (2) coupled between the first supply terminal and the pad; and a pull-down output device (3) coupled between the pad and the second supply voltage.

As to claim 6, it is inherent that the pull-up device has a gate coupled to a first predriver circuit (circuit, not shown, that generates the HI signal), and the pull-down device has a gate coupled to a second predriver circuit (circuit, not shown that generates the LO signal).

Claims 17-19 and 21 recites similar limitations of claims above. Therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US 2002/0017940) in view of Toyashima (US 20010017755).

Fujii et al.'s figure 5 shows all limitations of the claim except for a switch coupled between the pad and the clamp diode. However, Toyashima's figure 2 shows a circuit having switch F1 coupled between pad 10 and clamp diode D1 to remove the clamp circuit when circuit operates at high speed. Therefore, it would have been obvious to one having ordinary skill in the art to add switches between Fujji input pad and the diodes for the purpose of capable of increasing the circuit speed.

5. Claim 1-8, 17-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kan (US 2002/0057105) in view of Toyashima (US 20010017755).

As to claim 1, Kan's figure 1 shows a first integrated circuit (100) comprising: an input buffer (16) coupled between a first supply terminal and a second supply terminal and further

coupled to receive an input signal on a pad (17); and a resistor (20) coupled to the pad, and further coupled to receive an input signal. Thus, figure 1 shows all limitations of the claim except for a diode coupled between the pad and the first supply terminal. However, Toyashima's figure 2 shows a circuit having a protection circuit (D1, D2, F1, F2) for protecting the circuit breakdown. Therefore, it would have been obvious to one having ordinary skill in the art to add Toyashima's protection circuit to the input of Kan's input buffer 16 for the purpose of protecting the input buffer. Thus, the modified Kan's figure 1 further shows a clamp diode (Toyashima's D1) coupled between the pad and the diode.

As to claim 2, Kan's figure 1 further shows a second integrated circuit (200) coupled to the resistor and to provide the input signal.

As to claim 3, the modified Kan's figure 1 shows that clamp diode has a anode and a cathode, the anode is coupled to the pad, and the cathode is coupled to the first supply terminal.

As to claim 4, the modified Kan's figure 1 shows that the first supply terminal is configured to receive a positive supply voltage, and the second supply voltage is configured to receive a ground supply.

As to claim 5, the modified Kan's figure 1 shows that the integrated circuit further comprises: a pull-up output device (MP1) coupled between the first supply terminal and the pad; and a pull-down output device (MN1) coupled between the pad and the second supply voltage.

As to claim 6, the modified Kan's figure 1 shows that the pull-up device has a gate coupled to a first predriver circuit (31), and the pull-down device has a gate coupled to a second predriver circuit (32).

As to claim 7, it is inherent that the integrated circuit further comprises: a core (cirucit, not shown, that generates the OUTPUT DATA signal) comprising a plurality of logic gates, and one of the logic gates is coupled to provide a signal to the first predriver.

As to claim 8, he modified Kan's figure 1 shows a switch (Tayashima's F1) coupled between the pad and clamp diode.

Claims 17-19 and 21 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

6. Claim 9-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kan (US 2002/0057105) in view of Hirakata (JP 06-178445).

As to claim 9, Kan's figure 1 shows all limitations of the claim except for a series of clamp diodes coupled between the pad and the second supply terminal. However, Hirakata's figure 2 or 3 shows a plurality of clamp diodes (n2) coupled to the I/O line for protecting the IC (3). Therefore, it would have been obvious to one having ordinary skill in the art to add Hirakata's clamp diodes (n2) to the input of Kan's buffer for the purpose of protecting the buffer.

As to claim 10, the modified Kan's figure 1 shows that the series of clamp diodes comprises four diodes.

As to claim 11, the modified Kan's figure 1 shows a second integrated circuit (200) coupled to the resistor and to provide the input signal.

As to claim 12, the mofieid Kan's figure 1 shows that each of the clamp diodes in the series of clamp diodes has a anode and a cathode, the anode of one of the clamp diodes in the series of clamp diodes is coupled to the pad, and the cathode of one of the clamp diodes in the series of clamp diodes is coupled to the second supply terminal.

As to claim 13, the modified Kan's figure 1 shows that the first supply terminal is configured to receive a positive supply voltage, and the second supply voltage is configured to receive a ground supply.

As to claim 14, the modified Kan's figure 1 shows that the integrated circuit further comprises a pull-up output device (MP1) coupled between the first supply terminal and the pad; and a pull-down output device (MN1) coupled between the pad and the second supply voltage.

As to claim 15, the modified Kan's figure 1 shows that the pull-up device has a gate coupled to a first predriver circuit (31), and the pull-down device has a gate coupled to a second predriver circuit (32).

As to claim16, it is inherent that the integrated circuit further comprises:
a core comprising a plurality of logic gates (circuit, not shown, that generates the OUTPUT DATA signal), and one of the logic gates is coupled to provide a signal to the first predriver.

Claims 17-20 recites similar limitations of claims above. Therefore, they are rejected for the same reasons.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 3, 2005